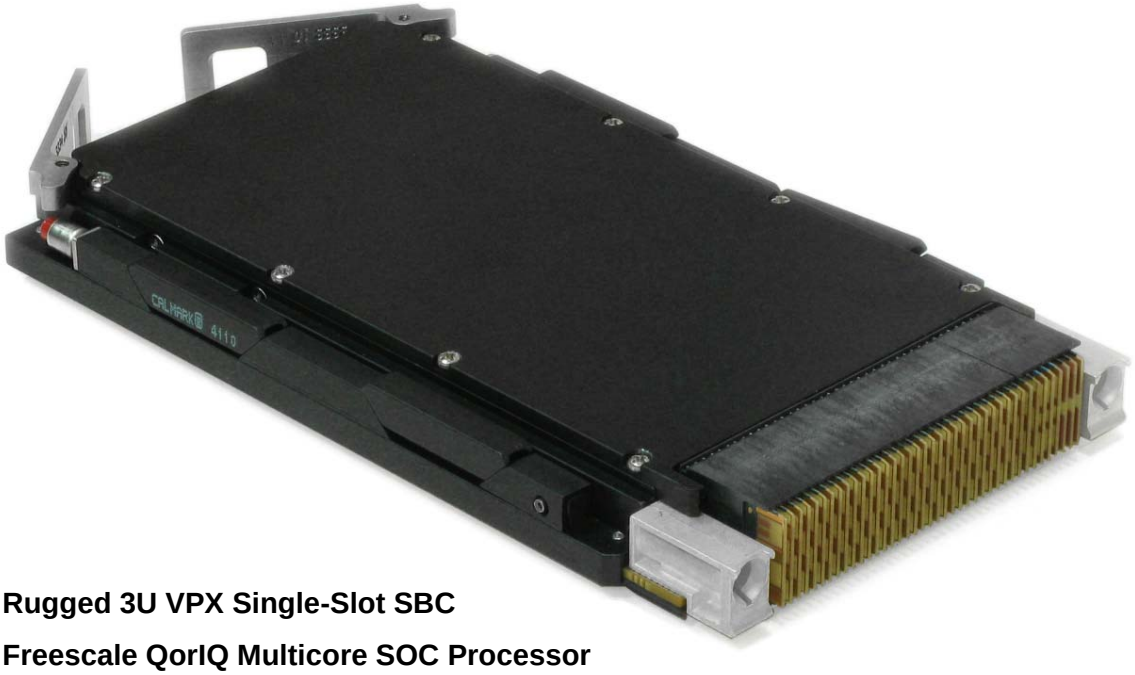
C912

Freescale™ QorIQ™ T4 3U VPX SBC



- Rugged 3U VPX Single-Slot SBC
- Freescale QorIQ Multicore SOC Processor
  - 8/4 e6500 Dual Thread Cores (T4160/T4080)
  - AltiVec Unit
- Memory Resources
  - 4 GB DDR3 SDRAM @ 1600 MT/s with ECC, in two banks
  - 256 MB NOR Flash Memory
  - Up to 16 GB SATA Flash Disk
  - 512 kB NVRAM (MRAM)
- I/O Interfaces
  - Two USB 2.0 Ports
  - Two SATA II Ports
  - Four Serial Channels
    - UART Operation
    - Support for RS-232/422 Physical Interface
    - Configurable for two serial with Modem Hardware Flow Control (RS-232 only)
  - 8 Discrete I/O Lines
- 4 Gigabit Ethernet Ports
- Multiple Backplane Interface Options
- VPX Core Fabric – Two 10 GbE(XAUI)/PCIe Gen2
- XMC Slot Supporting PCIe x4 Gen 2.0
- System Resources
  - Eight 32-Bit Timers
  - Standard and Windowed Watchdog Timers
  - Real Time Clock
  - Elapsed Time Recorder
  - On-Board Temperature Sensors
  - Intelligent Platform Management Interface (IPMI)
- RTOS Support
  - Wind River - VxWorks®
  - Green Hills - INTEGRITY®
  - Linux®
- OpenVPX Compliant
- Auto System/Peripheral Detection
- VITA 48 (REDI) Compliant Option
- Conduction and Air-Cooled Versions
- Vibration and Shock Resistant

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C912 – Freescale™ QorIQ™ T4 3U VPX SBC

The C912 is Aitech's new generation VPX PowerPC SBC based on Freescale's new T4 Series QorIQ System-on-Chip (SoC) multi-thread processors, with on-chip high speed L1 and L2 caches, and numerous integrated bus, memory, and I/O controllers.

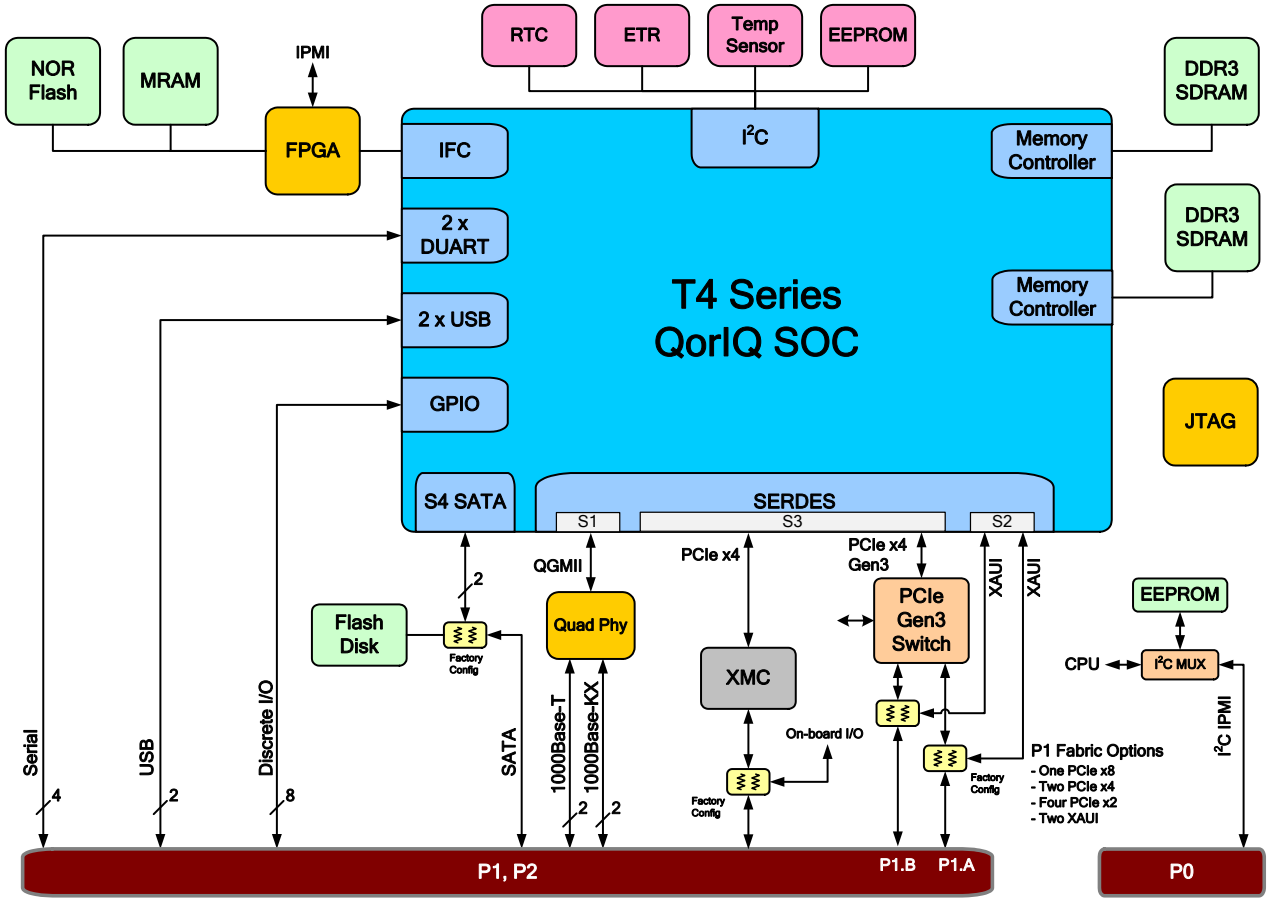
C912 memory resources include large and fast DDR3 SDRAM, User and Boot NOR Flash for firmware, user application, and data storage, MRAM for user/application specific parameter storage, and a high-density NAND Flash disk for mass storage.

Integrated on-board I/O resources include Gigabit Ethernet, USB 2.0 ports, SATA II, serial ports, and general-purpose discrete I/O channels.

The C912 is VPX compliant per VITA 46 and VITA 65, and is capable of communicating with up to four other PCIe VPX boards, eliminating the need for another switch in the system.

To complement its extensive capabilities and provide extended resources and flexibility, the C912 is equipped with an industry standard XMC slot.

The C912 is available in air-cooled and conduction-cooled versions.



C912 Block Diagram

Functional Description

Board Architecture

The C912 is a single slot 3U VPX SBC designed around Freescale's T4 Series QorIQ System-on-Chip (SOC) processors, combining a powerful processing platform with extensive I/O capabilities.

QorIQ Multi-core System on Chip (SoC)

The QorIQ Soc delivers an I/O intensive state-of-the-art package combining 8 (T4160) or 4 (T4080) cores with dual DDR3 memory controllers, PCIe, SRIO, DMA, SATA, USB, Ethernet, and local device I/O. The QorIQ SoC includes on-chip 32k/32k (I/D) L1 and 2 MB shared L2 caches.

With differing numbers of processing cores, the two processor options enable system designers to select a C912 configuration (see Ordering Information) with the optimum combination of processing power and power consumption for their system designs. Other than the number of cores, all SoC features and parameters described in this datasheet are the same for the T4160 and T4080 QorIQ SoC processors.

QorIQ SoC Performance

The QorIQ T4 Series Advanced Multicore Processor combine up to 8 dual-threaded e6500 Power Architecture processor cores with the high-performance data path acceleration logic and network and peripheral bus interfaces required for mil/aerospace applications.

QorIQ SoC Cores

Each high-performance 64-bit Power Architecture Book E-compliant e6500 core supports two hardware threads, each of which appears to application software as a virtual CPU. The e6500 CPUs are arranged in clusters of four, with a shared a 2 MB L2 cache.

VPX Capabilities

The C912 supports several interfaces including XAUI, PCIe, 1000Base-KX, and 1000Base-TX Ethernet ports. Refer to the *Backplane Fabric Options* table for a complete summary of the C912 VPX capabilities.

VPX Data Plane (P1) Fabric Interfaces

The C912 supports 2-port/4-lane (x4) serial switch fabric on P1, to allow connectivity to other VPX agents (payload and expansion cards) in the system. The switch fabric interface supports one or two ports (DP1-DP2) configurable as XAUI or PCIe (factory configuration).

XAUI (VITA 46.7 compliant) is a standard for a 10 Gb Media Independent Interface between the 10 Gigabit Ethernet (10 GbE) MAC and PHY layers.

PCIe (VITA 46.4 compliant) is suited to connecting with PCIe and PCI-based peripheral devices.

VPX Control Plane (P1) Switch Support

The C912 is capable of connecting to a switch slot per VITA 46.9 by routing two 1000Base-KX and two 1000Base-T Ethernet ports to P1, enabling the designer to connect those ports to a switch slot per VITA 46.20.

VPX Expansion Plane (P1)

The C912 connects a PCIe (VITA 46.4 compliant) port/4-lane (x4) serial switch fabric on P1, to allow connectivity to other VPX agents (payload and expansion cards) in the system. The switch fabric interface is suited to connecting with PCIe based peripherals.

OpenVPX Slot Profile

The C912 supports the following slot profiles (see *Ordering Information*) as defined in the OpenVPX specification (VITA 65):

- SLT3-PAY-2F2U-16.2.3-n
- SLT3-PAY-2F2T-16.2.5-n

The SLT3-PAY-2F2U-16.2.3-n option is software configurable to support the following additional Data Plane configuration.

- SLT3-PAY-1F1F2U-16.2.4-n
- SLT3-PAY-2F-16.2.7-n
- SLT3-PAY-1F2U-16.2.11-n
- SLT3-PAY-1D-16.2.6-n

VPX System Management

System level management monitoring of board health status information (e.g. rail voltages, board temperatures, etc.) is available over the VPX connectors via the I^2C bus at P0. The system management unit is powered by the VPX +3.3 Vdc Auxiliary power supply and is available even in the event of board failure or power loss.

VPX REDI (VITA 48)

The conduction-cooled C912 is optionally offered in a VPX REDI compliant version, supporting two-level maintenance per VITA 48, with top and bottom covers shielding the complete C912 assembly including installed XMC module.

Memory

The C912 is equipped with large memory arrays to compliment and support the high processing power.

SDRAM

A total of 4 GB of DDR3 SDRAM operating at 1600 MT/s, is provided in two banks. Each bank is controlled by a dedicated memory controller integrated in the QorIQ SoC processor.

The DDR3 SDRAM arrays are ECC protected guarantying high data integrity.

Boot/User Flash

Boot and User Flash on the C912 are implemented in a 256 MB NOR Flash memory device. 64 MB is allocated as Boot Flash for Aitech proprietary firmware storage. Boot Flash employs protection measures to assure boot code protection. 192 MB of the NOR Flash is fully available to the user for application storage, data logging, file system mounting and any other use required.

NVRAM

512 kB of NVRAM memory is provided by an MRAM device. MRAM technology provides non-volatile memory with unlimited writes, fast access, and long term data retention while powered down. NVRAM is available for application specific parameter storage and logging purposes.

Flash Disk

A SATA II Flash Disk of up to 16 GB provides on-board mass storage, eliminating the need for externally attached storage media.

I/O Interfaces

The C912 offers a diverse I/O feature set including Ethernet, SATA II, USB 2.0, serial ports, and discrete channels. These interfaces allow attachment of a wide range of peripherals to the C912, including sensors, communication devices, storage media, pointing devices, and others.

Ethernet

The C912 is equipped with up to four Gigabit Ethernet ports, all implemented in the QorIQ SOC processor, with an external PHY device.

Two 1000Base-KX and two 1000Base-T Ethernet ports are routed to the backplane connectors.

Serial I/O

The C912 includes four standard asynchronous UART-based serial ports, provided directly by the QorIQ SoC processor, and supporting RS-232/422.

Serial ATA (SATA) II

The on-board SATA controller, integrated in the QorIQ SoC processor, provides two SATA II ports. On boards equipped with an on-board Flash Disk, one of these ports provides the interface for it, and the other is routed to the backplane I/O connector. On boards with no on-board Flash Disk, both SATA interfaces are routed to the backplane connector.

Discrete I/O

The C912 is equipped with up to 8 single-ended or 4 differential general-purpose Discrete I/O channels. The Discrete I/O controller is integrated in the QorIQ SoC . The channels can be independently set for single-ended operation or as pairs for differential RS-422 operation. Each of the channels can be independently configured as input or output. When configured as input, each of these channels may be programmed to generate an interrupt on any level shift event.

USB

The QorIQ SoC provides two USB 2.0 controllers with integrated PHY providing point-to-point connectivity that complies with the USB specification, Rev. 2.0.

The USB transceivers support high-speed, full-speed, and low-speed signaling.

Both USB interfaces are routed to the backplane connectors.

XMC Expansion Slot

The C912 provides an industry standard XMC expansion slot for extended flexibility and integration of additional elements to the SBC.

The XMC slot is interconnected to the QorIQ SoC via 4-lane (x4) PCIe port.

XMC site PCIe bus operation (speed, number of lanes) is automatically configured according to the capabilities of the installed XMC module.

The following table summarizes XMC site capabilities and characteristics:

PCIe Interface	x4
XMC I/O routing (P16)	VITA 46.9
Max current available from +5 Vdc	3 A
Max current available from +3.3 Vdc	2 A
+12 Vdc_{AUX}	0.5 A
-12 Vdc_{AUX}	0.5 A
Power per site (max)	10 W

Transition Module

For convenient connection to the C912's multiple I/O interfaces, Aitech offers the TM912 transition module.

The TM912 provides easy access to all C912 on-board and XMC I/O interfaces through industry standard connectors. The TM912 may be installed in air-cooled chassis supporting rear plug-in units.

For more information on the TM912, refer to its product datasheet.

System Resources

General-Purpose Timers

The C912 provides two groups of four global 32-bit timers clocked with the MPIC input clock (333 MHz) with 8, 16, 32 and 64 dividing options. The timers can also be clocked using the RTC clock (3.125 MHz).

Timers within each group can be concatenated to time longer durations.

Real Time Clock

A Real-Time Clock (RTC) provides time and date storage. In the event of power loss, the RTC automatically switches to the backup source, utilized through a super capacitor. The super capacitor (electrolytic) enables data storage while board power is down. The RTC includes a trickle charging circuit that loads the capacitor while on-board power is present.

Standard Watchdog Timers

Each QorIQ thread incorporates a watchdog timer that generates a timeout event when not serviced before the programmed time interval expires.

Windowed (Avionics) Watchdog Timer

The C912 provides a programmable windowed watchdog timer that is integrated in its on-board PLD. The windowed watchdog timer generates a timeout event if the timer is serviced before or after the allowed window.

Each of the two timers (standard and windowed watchdog) may be independently set to generate a non-maskable interrupt or to reset the SBC.

Elapsed Time Recorder

An on-board electronic Elapsed Time Recorder (ETR) records cumulative operation time and power on-off cycles in a dedicated NVRAM whenever the C912 is powered. ETR data is software accessibly by the user.

Temperature Sensors

The C912 contains three temperature sensors. One sensor is integrated in the QorIQ SoC processor to provide die temperature, and the other two are located adjacent to the card edges.

Status Indicators

Four hardware debug LEDs and four software debug LEDs are available on the C912 for diagnostics and debugging purposes.

Software

The C912 is delivered with a comprehensive software package allowing the user to take full advantage of the SBC's capabilities.

Firmware Features

An extensive pre-burned firmware suite comprises several software entities providing the firmware infrastructure of the board.

Startup firmware is based on the open source U-Boot boot loader, and provides the following capabilities:

- Power-up sequence control
- Boot loader capabilities supporting various boot devices and file formats
- Hardware debugging tool
- Power-up BIT

Diagnostics, designed in a Linux environment, provide a powerful testing and verification tool.

The C912 provides a COP/JTAG interface for debugging and development purposes.

OS/RTOS Support

The C912 is supported by several OS (Operating System) and RTOS (Real-Time Operating System) platforms for which complete BSPs (Board Support Packages) are available. These platforms include:

- Linux for PowerPC (based on FSL SDK)
- Wind River VxWorks
- Green Hills INTEGRITY®
- Other RTOS BSPs may be available upon request.

Each BSP includes a set of drivers and utilities.

Mechanical Features

Features & Dimensions

- Air-cooled per ANSI/VITA 46.0
- Conduction-cooled per ANSI/VITA 46.0
- Conduction-cooled REDI: per VITA 48.2

All mechanical formats are single slot 3U modules.

A custom metal frame provides excellent rigidity and shock resistance, as well as an array of stiffeners to support a rugged XMC.

Weight

Weights in grams (lbs) of the various C912 mechanical configurations (see *Ordering Information* below) are listed in the following table.

Cooling + Pitch		
A3	**R0**	**R2**
<400 (0.88)	<780 (1.2)	<860 (1.9)

Mechanical Design & Thermal Management

C912 Air-Cooled

The air-cooled rugged C912 fully complies with ANSI/VITA 46.0. The mechanical/thermal design includes a reinforced front panel and a finned metal heatsink/rugged stiffening frame for improved thermal and mechanical properties.

The air-cooled XMC site is ready for installation of an air-cooled XMC module that complies with IEEE STD 1386-2001 and ANSI/VITA 42.3 respectively.

The front panel is equipped with an aluminum extraction handle suitable for VPX stresses, and with an opening for the XMC front panel.

The C912 air-cooled version is available in 1" pitch (slot spacing) only.

C912 Conduction-Cooled

The C912 employs a sophisticated mechanical design based on Aitech's many years of rugged SBC design experience. This design allows for optimal heat conduction across the board and heat rejection from the card edges. This design also ensures rigidity and endurance under extreme environmental conditions.

The conduction-cooled rugged C912 fully complies with ANSI/VITA 46.0. It includes a robust metal heatsink with built-in stiffening ribs. The geometry of the heatsink ensures efficient heat conduction to the side rails. A reverse thermal interface coupled with wedgelocks secure the board firmly in place and ensures good thermal contact with the chassis for effective heat transfer. This mechanical structure is extremely durable and particularly suited to the on-board high power components. The C912 also complies with ANSI/VITA 48.2 (REDI) supporting Two Level Maintenance. This is achieved through additional covers for the SBC bottom and over the XMC module. This structure also creates a closed faraday cage structure, for superior EMI/RFI performance. Board extractors integral to the heatsink facilitate removal of the board from its enclosure.

For high efficiency cooling, the CPU and other high power components are located near the card edges for short thermal paths to the chassis sidewalls. Component locations in combination with heatsink design result in balanced heat dissipation via the two card edges.

The XMC site is available for hosting conduction-cooled rugged XMC modules that comply with ANSI/VITA 42.0. The XMC site provides a conduction path from the XMC primary thermal interface to the C912 metal heatsink for cooling of the mezzanine. A removable rib provides an additional heat transfer path for XMC modules that have a secondary thermal interface.

The conduction-cooled board has no front panel; all XMC I/O signals are directed to the VPX backplane connectors.

The standard conduction-cooled C912 is available in 0.85” pitch; the REDI version is available in 1” pitch.

Power Requirements

The C912 takes all its power from the VPX backplane. It should be provided with +5.0 V, +3.3 V, +3.3V_AUX, and ±12 V_AUX as defined by the VPX specification (-12 V_AUX is required for XMC compliance only; the C912 does not require -12 V_AUX for its own operation).

All other power sources required by C912 resources are generated on-board.

The XMC site is provided with either +5 V or +12 V VPWR. The default power is 5 V.

All other power sources required by C912 resources are generated on board.

Total power consumption of the C912 depends on its configuration and assembly options.

In its fully featured configuration (no XMC installed), C912 power consumption, is as follows:

Processor	Typical
T4080 @ 1.5 GHz	TBD W
T4160 @ 1.5 GHz	TBD W

Environmental Features

Please refer to the Aitech Ruggedization datasheet.

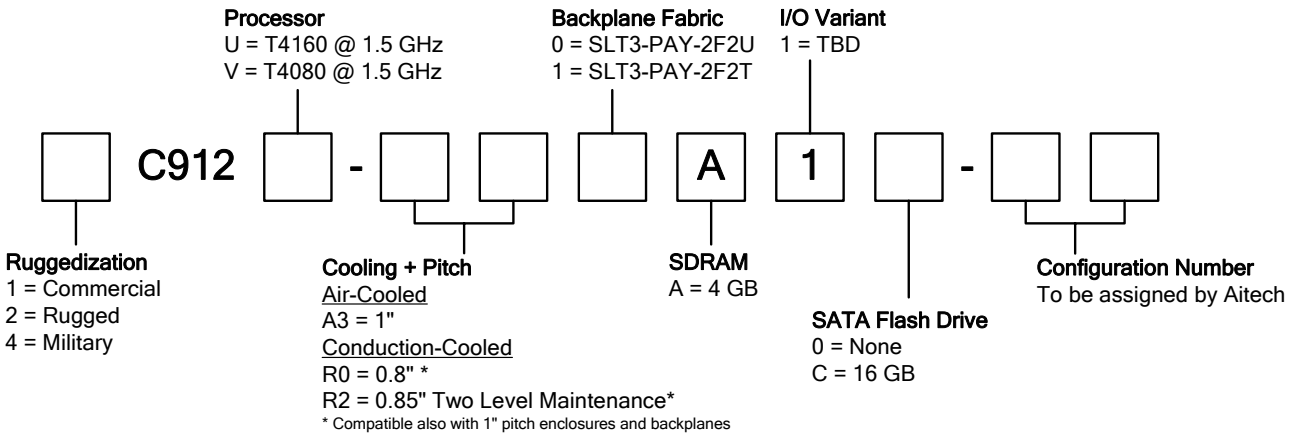
C912

Freescale™ QorIQ™ T4 3U VPX SBC

I/O Variants

TBD

Ordering Information



Example: 4C912U-R01A1C-00

C912 Backplane Fabric Options

Option #	P1 (Data Plane)		P1 (Expansion Plane)	P1 (Control Plane)				P2 (I/O)	VITA 65 Profile Name
	4-lane	4-lane		1000Base-KX		1000Base-T			
	DP1	DP2		CPutp1	CPutp2	CPtp1	CPtp2	Gb Port	
1	XAUI	XAUI	-	Up to 2 ports in any combination				Up to 2 *	SLT3-PAY-2F2U-16.2.3-n
2	PCIe	PCIe	-						
3	PCIe	-	PCIe x4						SLT3-PAY-2F2T-16.2.5-n
9	Custom								

* I/O Variant dependent

For more information about the C912 or any Aitech product, please contact Aitech Defense Systems sales department at (888) Aitech-8 (248-3248).

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