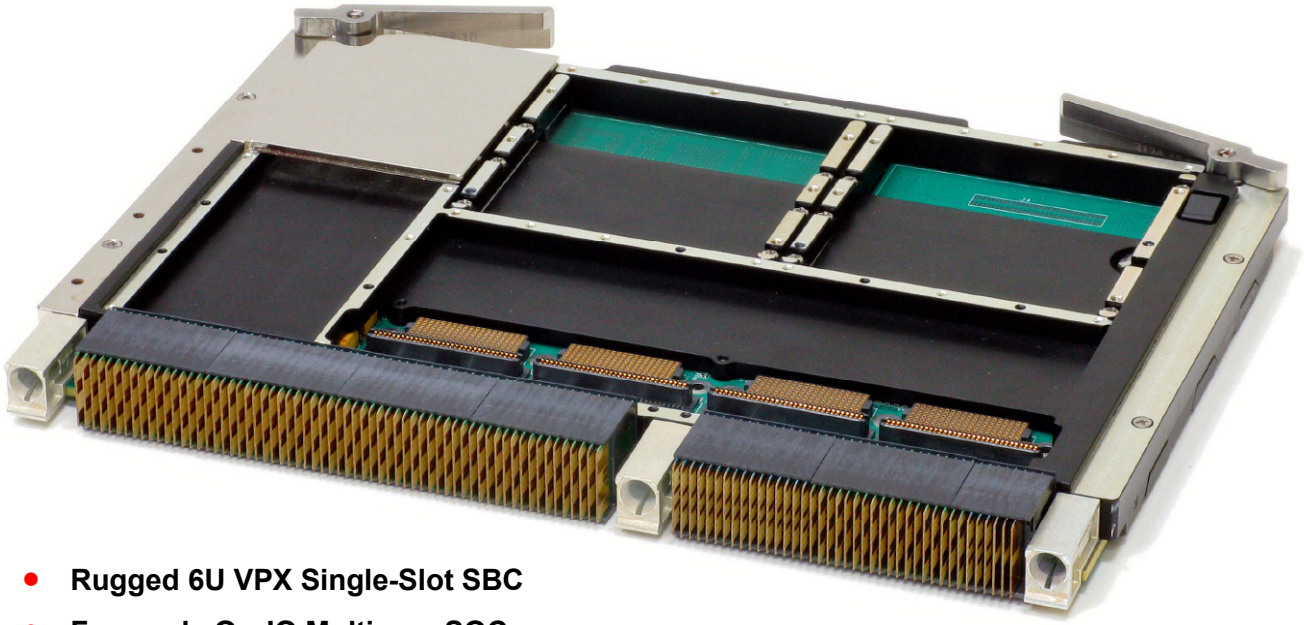
C112

Freescale™ QorIQ™ T4 6U VPX SBC



- Rugged 6U VPX Single-Slot SBC
- Freescale QorIQ Multicore SOC
  - 12/8 e6500 Dual Thread Cores (T4240/T4160)
  - AltiVec Unit
- Memory
  - Up to 8 GB DDR3 SDRAM @ 1600 MT/s with ECC (Dual Channel, 4 GB each)
  - 256 MB NOR Flash Memory
  - 16 GB Flash Disk Mass Storage
  - 512 kB NVRAM (MRAM)
- I/O Interfaces
  - SATA 2.0 Port
  - Two USB 2.0 Ports
  - Serial Ports supports RS232\RS422\RS485
    *Four multi-Protocol High-Speed Serial
    *Six standard UARTs
  - Two Dual Redundant MIL-STD-1553B Ports
  - 16 Single-Ended / 8 Differential RS-422 Discrete I/O Lines
- Multiple Backplane Interface Options
- VPX Core Fabric – 10GbE(XAUI)\PCIe Gen2\SRIO
- Up to 6 Gigabit Ethernet Ports
- Expandability
  - 2 PMC/XMC Sites Supporting PCI/PCI-X 64-bit up to 133 MHz and PCIe x8
- System Resources
  - Eight 32-Bit Timers
  - Standard and Windowed Watchdog Timers
  - Real Time Clock
  - Elapsed Time Recorder
  - On-Board Temperature Sensors
- 5 V or 12 V Operation
- RTOS Support
  - Wind River - VxWorks®
  - Green Hills - INTEGRITY®
  - Linux®
- OpenVPX Compliant
- VITA 48 (REDI) Compliant Option
- Conduction and Air-Cooled Versions
- Vibration and Shock Resistant

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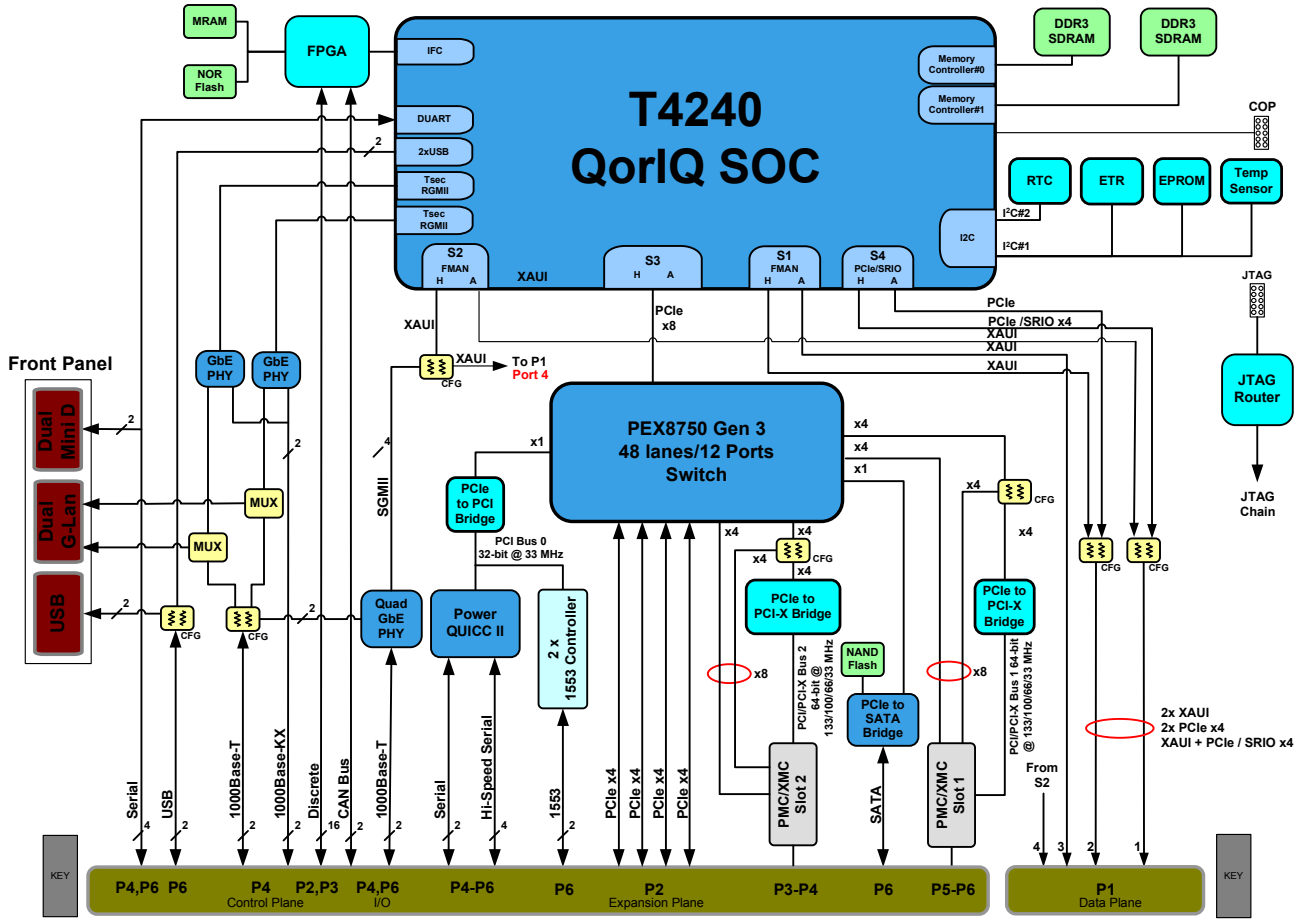


C112 Block Diagram

The C112 is the new generation Aitech PowerPC based product targeting the new VPX (VITA 46.0) and OpenVPX (VITA 65) platforms.

At the heart of the C112 is Freescale's new T4240 QorIQ System-on-Chip (SOC) 12 core processor, with its on-chip high speed L1 and L2 caches, and numerous integrated bus, memory, and I/O controllers.

C112 memory resources include large and fast DDR3 SDRAM, NOR Flash for firmware, user application, and data storage, MRAM for user/application specific parameter storage, and a high-density NAND Flash array for mass storage.

Integrated on-board I/O resources include Gigabit Ethernet, USB 2.0 ports, MIL-STD-1553, SATA II, serial ports, and general-purpose discrete I/O channels.

To complement its extensive capabilities and provide extended resources and flexibility, the C112 is equipped with two industry PMC/XMC slots.

The C112 mechanical and electrical design guarantees its operation over the full range of rugged application environments. It is available in industry standard 0.85" pitch conduction-cooled or 1" pitch air-cooled form factors. The 0.85" pitch conduction-cooled version is also available in the VITA 48 (VPX REDI) format with covers to support two level maintenance LRM requirements.

Functional Description

Board Architecture

The C112 is a single slot 6U VPX SBC designed around Freescale's 12-core T4240 QorIQ System-on-Chip (SOC), combining a powerful processing platform with extensive I/O capabilities.

T4240 Multi-core System on Chip (SoC)

The T4240 delivers an I/O intensive state-of-the-art package combining 12 cores with dual DDR3 memory controllers, PCIe, SRIO, DMA, SATA, USB, Ethernet, and local device I/O. Operating at up to 1.67 GHz, the T4240 includes on-chip 32k/32k (I/D) L1 and 2 MB shared L2 caches per cluster.

For power sensitive applications, the C112 is available with a low power version of the T4240, operating at 1.5 GHz or an 8 core T4160 operating at 1.5 GHz (see ordering information).

T4240 Performance

The QorIQ T4240 Advanced Multicore Processor combines 12 dual-threaded e6500 Power Architecture processor cores (8 cores for the T4160) with the high-performance data path acceleration logic and network and peripheral bus interfaces required for mil/aerospace applications.

As Freescale's current flagship QorIQ multicore SoC, the T4240 delivers approximately four times the computing horsepower of the P4080.

T4240 Cores

Each high-performance 64-bit Power Architecture Book E-compliant e6500 core supports two hardware threads, each of which appears to application software as a virtual CPU. The e6500 CPUs are arranged in clusters of four, with a shared 2 MB L2 cache.

VPX Capabilities

The C112 supports several interfaces like XAUI, PCIe, S-RIO, 1000Base-KX, 1000Base-TX Ethernet ports. Table 3summarizes the C112 VPX capabilities:

VPX Data Plane (P1) Fabric Interfaces

The C112 supports 4-port/4-lane (x4) serial switch fabric on P1, to allow connectivity to other VPX agents (payload and expansion cards) in the system. The switch fabric interface supports four ports (DP1-DP4) configurable as XAUI/SRIO or PCIe (factory configuration).

XAUI (VITA 46.7 compliant) is a standard for a 10 Gb Media Independent Interface between the 10 Gigabit Ethernet (10 GbE) MAC and PHY layers.

PCIe (VITA 46.4 compliant) is suited to connecting with PCIe and PCI-based peripheral devices, while SRIO (VITA 46.3 compliant) is ideal for processor to processor communications.

Note: When choosing T4160 QorIQ SOC, PCIe interfaces in port 2 or XAUI in port 3 will not be available. Refer to Table 3 for the availability options.

VPX Control Plane (P4) Switch support

The C112 is capable of connecting to a switch slot per VITA 46.9 by routing two 1000Base-KX and two 1000Base-T Ethernet ports to P4, enabling the designer to connect those ports to a switch slot per VITA 46.20.

VPX Expansion Plane (P2)

The C112 connects 4 PCIe (VITA 46.4 compliant) port/4-lane (x4) serial switch fabric on P2, to allow connectivity to other VPX agents (payload and expansion cards) in the system. The switch fabric interface is suited to connecting with PCIe based peripheral

OpenVPX Slot Profile

The C112 supports the following slot profiles (see ordering information) as defined in the OpenVPX specification (VITA 65):

- MOD6-PAY-4F2T-12.2.2-n
- MOD6-PAY-2F2U2T-12.2.5-n

VPX System Management

System level management monitoring of board health status information (e.g. rail voltages, board temperatures, etc.) is available over the VPX connectors via the I^2C bus at P0. The system management unit is powered from the VPX +3.3 Vdc Auxiliary power supply and is available even in the event of board failure or power loss.

VPX REDI (VITA 48)

The conduction-cooled C112 is optionally offered in a VPX REDI compliant version, supporting two-level maintenance per VITA 48, with top and bottom covers shielding the complete C112 assembly including installed PMC/XMC modules.

Memory

The C112 is equipped with large memory arrays to compliment and support the high processing power.

SDRAM

A total of 8 GB of DDR3 SDRAM, operating at 1600 MT/s, is provided in two banks. Each bank is controlled by a dedicated memory controller integrated in the T4240.

The DDR3 SDRAM arrays are ECC protected guarantying high data integrity.

Boot/User Flash

Boot and User Flash on the C112 are implemented in a 256 MB NOR Flash memory device. 64 MB is allocated as Boot Flash for Aitech proprietary firmware storage. Boot Flash employs protection measures to

assure boot code protection. 192 MB of the NOR Flash is fully available to the user for application storage, data logging, file system mounting and any other use required.

NVRAM

512 kB of NVRAM memory is provided by an MRAM device. MRAM technology provides non-volatile memory with unlimited writes, fast access, and long term data retention while powered down. NVRAM is available for application specific parameter storage and logging purposes.

Flash Disk

An on-board 16 GB SATA II Flash Disk provides mass storage capability, eliminating the need for externally attached mass-storage media. The Flash Disk is controlled directly by the on-board SATA controller.

I/O Interfaces

The C112 offers a diverse I/O feature set including Ethernet, SATA II, USB 2.0, serial ports, MIL-STD-1553B and discrete channels. These interfaces allow attachment of a wide range of peripherals to the C112, including sensors, communication devices, storage media, pointing devices, and other peripherals.

Ethernet

The C112 is equipped with up to six Gigabit Ethernet ports all implemented within the T4240, operation with external PHY devices. Two 1000Base-KX and two 1000Base-T Ethernet ports are routed to the control plane (P4). Additional two 1000Base-T are routed as I/Os to P4 and P6 to the control plane (P4)

In air-cooled versions, two of the Ethernet ports are software configurable to be routed to front panel RJ-45 connectors.

Serial I/O

The C112 provides ten serial ports supporting RS-232/422/485 physical interfaces.

Four of these channels are high-speed multi-protocol synchronous/asynchronous ports supporting all common serial communications protocols (UART, USART, SDLC, HDLCetc.) The serial channels are implemented using a PowerQUICC II communications processor residing on a 66 MHz PCI bus to allow high-speed operation and high throughput of the serial channels. Each of the PowerQUICC II serial channels is controlled through an SCC coupled with its SDMA (Serial DMA) engines and operating with minimal host processor intervention.

The remaining six serial ports implement standard asynchronous UART-based ports. Two are from the PowerQUICC II SMC UARTs and the other four are provided directly from the T4240.

Serial ATA (SATA) II

The on-board SATA controller provides two SATA II ports (with backward compatibility to SATA 1.0). One port is routed to the backplane I/O connector while the second port is assigned for the on-board Flash Disk.

The SATA II controller utilizes a PCIe to SATA Bridge integrating the SATA link and the PHY. The SATA Bridge connects via a 1-lane (x1) PCIe bus and provides a transfer rate of 3.0 Gb/s (may be limited due to PCIe bandwidth).

Discrete I/O

The C112 is equipped with up to 16 single-ended or 8 differential general-purpose Discrete I/O channels. The Discrete I/O controller is integrated in the C112 FPGA. The channels can be independently set for single-ended operation or as pairs for differential RS-422 operation. Each of the channels can be independently configured as input or output. Configured as input each of these channels may be programmed to generate an interrupt on any level shift event.

T4240 USB

The T4240 provides two USB 2.0 controllers with integrated PHY provide point-to-point connectivity that complies with the USB specification, Rev. 2.0.

The USB transceivers support high-speed, full-speed, and low-speed signaling.

Air-cooled versions provide one USB port at the front panel, while in the conduction cooled version the ports routed to backplane connectors.

MIL-STD-1553B

The C112 provides two on board dual redundant MIL-STD-1553B ports, implemented using two DDC PCI controllers. Each of the controllers is capable of BC or Multi RT with Concurrent Bus Monitor.

The MIL-STD-1553B controllers support 66 MHz PCI operation and DMA engine.

Expansion Slots

PMC/XMC Sites

The C112 provides two industry standard PMC/XMC expansion sites for extended flexibility and integration of additional elements to the SBC. Each of the sites is capable of operating as PMC or XMC.

PMCs: Each of the PMC slots is interconnected to the SBC main PCI switch through a PCIe-PCI-X Bridge. This PCI bus supports PCI-X operation at 133/100/66 MHz and PCI operation at 33/66 MHz bus depending on PMC capabilities.

Both PMC slots are capable of hosting PMCs with 3.3 V or 5 V PCI signaling levels. The keying for both slots is universal (no key).

XMCs: Each of the XMC slots is interconnected to the SBC main PCIe switch through 8-lane (x8) port.

An on-board logic control module probes the two PMC/XMC sites and automatically sets PCI/PCI-X or PCIe operation mode as well as PCI bus frequency according to XMC/PMC presence and PMC operation mode/frequency capabilities.

The following table summarizes PMC/XMC site capabilities and characteristics:

Table 1. C112 PMC/XMC Site Capabilities

	PMC/XMC 1	PMC/XMC 2
Location	Inner Site	Outer Site
PCIe Interface	x8	x8
PCI Interface (max)	PCI-X 133 Mhz	
PCI I/O Signaling Levels	Universal (3.3 V/5V)	
PMC I/O routing (Pn4)	VITA 46.9 PMC/XMC I/O Multiplexed	
XMC I/O routing (Pn6)		
Max current available from +5 Vdc (PMC/XMC)	2 A/3 A	2 A/3 A
Max current available from +3.3 Vdc	2 A	2 A
+12 Vdc_{AUX}	0.5 A	0.5 A
-12 Vdc_{AUX}	0.5 A	0.5 A
Power per site (max)	10 W	20 W

PMC/XMC I/O Routing

PMC/XMC I/O routing on the C112 supports the I/O routing configurations as defined by VITA 46.9.

Transition Module

For convenient connection to the C112's multiple I/O interfaces, Aitech offers the TM112 transition module.

The TM112 provides easy access to all C112 on-board and PMC/XMC I/O interfaces through industry standard connectors. The TM112 may be installed in air-cooled chassis supporting rear plug-in units.

For more information on the TM112, refer to its product datasheet.

System Resources

General-Purpose Timers

The C112 provides two groups of four global 32-bit timers clocked with the MPIC input clock (333 MHz) with 8, 16, 32 and 64 dividing options. The timers can also be clocked using the RTC clock (3.125 MHz).

Timers within each group can be concatenated to time longer durations.

Real Time Clock

A Real-Time Clock (RTC) provides time and date storage. In the event of power loss, the RTC automatically switches to the backup source, utilized through a super capacitor. . The super capacitor (electrolytic) enabling data storage while board power is down. The RTC includes a trickle charging circuit that loads the capacitor while on-board power is present.

Standard Watchdog Timers

Each QorIQ thread incorporates a watchdog timer that generates a timeout event when not serviced before the programmed time interval expires

Windowed (Avionics) Watchdog Timer

The C112 provides a programmable windowed watchdog timer that is integrated in its on-board PLD. The windowed watchdog timer generates a timeout event if the timer is serviced before or after the allowed window.

Each of the two timers (standard and windowed watchdog) may be independently set to generate a non-maskable interrupt or to reset the SBC.

Elapsed Time Recorder

An on-board electronic Elapsed Time Recorder (ETR) records cumulative operation time and power on-off cycles in a dedicated NVRAM whenever the C112 is powered. ETR data is software accessibly by the user.

Temperature Sensors

The C112 contains five temperature sensors. Two sensors are integrated in the T4240 to provide die temperatures, and the other three are located adjacent to the two card edges.

Status Indicators

Four hardware debug LEDs and four software debug LEDs are available on the C112 for diagnostics and debugging purposes.

In its air-cooled version the C112 includes two additional status indicators at the front panel. One is a primary/auxiliary power indicator and the second is user programmable.

Front Panel Connectors and Switches

In its air-cooled version the C112 has a front panel with the following features:

- Mini D-Type connector delivering two serial ports
- Two RJ45 connector delivering two GbE ports *
- Type-A USB connector delivering one USB port *
- Abort/Reset push-button
- Two Status Indicator LEDs

* Front panel I/Os are at the expense of rear I/Os

Software

The C112 is delivered with a comprehensive software package allowing the user to take full advantage of the SBC's capabilities.

Firmware Features

An extensive pre-burned firmware suite comprises several software entities providing the firmware infrastructure of the board:

Startup firmware is based on the open source U-Boot boot loader, and provides the following capabilities:

- Power-up sequence control
- Boot loader capabilities supporting various boot devices and file formats
- Hardware debugging tool
- Power-up BIT

Diagnostics, designed in a Linux environment, provide a powerful testing and verification tool

The C112 provides a COP/JTAG interface for debugging and development purposes.

OS/RTOS Support

The C112 is supported by several OS (Operating System) and RTOS (Real-Time Operating System) platforms for which complete BSPs (Board Support Packages) are available. These platforms include:

- Linux (various distributions)
- Wind River VxWorks 6.7
- Other RTOS BSPs may be available upon request.

Each BSP includes a complete set of drivers and utilities supporting all on board resources including inter-processor communication capabilities.

Mechanical Features

The C112 is available in the following mechanical formats.

Features & Dimensions

- Air-cooled per ANSI/VITA 46.0
- Conduction-cooled per ANSI/VITA 46.0
- Conduction-cooled REDI: per VITA 48.2

All mechanical formats are single slot 6U modules.

A custom metal frame provides excellent rigidity and shock resistance, as well as an array of stiffeners to support rugged PMCs/XMCs.

Weight

- Air-cooled: < 1200 g (2.7 lbs)
- Conduction-cooled: < 1350 g (3.0 lbs)
- Conduction-cooled REDI: < 1400 g (3.1 lbs)

All mechanical formats are single slot 6U modules.

Mechanical Design & Thermal Management

C112 Air-Cooled

The air-cooled rugged C112 fully complies with ANSI/VITA 46.0. The mechanical/thermal design includes a reinforced front panel and a finned metal heatsink/rugged stiffening frame for improved thermal and mechanical properties.

The two air-cooled PMC/XMC sites are ready for installation of air-cooled PMC and XMC modules that comply with IEEE STD 1386-2001 and ANSI/VITA 42.3 respectively.

The front panel is equipped with two aluminum extraction handles suitable for VPX stresses, and with openings for the two PMC/XMC front panels.

The C112 in its air-cooled version is available in 1" pitch (slot spacing) only.

C112 Conduction-Cooled

The C112 employs a sophisticated mechanical design based on Aitech's many years of rugged SBC design experience. This design allows for optimal heat conduction across the board and heat rejection from the card edges. This design also ensures rigidity and endurance under extreme environmental conditions.

The conduction-cooled rugged C112 fully complies with ANSI/VITA 46. It includes a robust metal heatsink with built-in stiffening ribs. The geometry of the heatsink ensures efficient heat conduction to the side rails. A reverse thermal interface coupled with wedgelocks secure the board firmly in place and ensures good thermal contact with the chassis for effective heat transfer. This mechanical structure is extremely durable and particularly suited to the on-board high power components. The C112 also complies with ANSI/VITA 48.2 (REDI) supporting Two Level Maintenance. This is achieved through additional covers for the SBC bottom and over the PMC/XMC modules. This structure also creates a closed faraday cage structure, for superior EMI/RFI performance. Board extractors integral to the heatsink facilitate removal of the board from its enclosure.

For high efficiency cooling, the CPU and other high power components are located near the card edges for short thermal paths to the chassis sidewalls. Component locations in combination with heatsink

design result in balanced heat dissipation via the two card edges.

The two PMC/XMC sites are available for hosting conduction-cooled rugged PMC and XMC modules that comply with ANSI/VITA 20-2001 and ANSI/VITA 42.3 respectively. The PMC/XMC sites provide a conduction path from the PMC/XMC primary thermal interfaces to the C112 metal heatsink for cooling of the mezzanines. Two removable ribs provide an additional heat transfer path for PMC/XMC modules having a secondary thermal interface.

The conduction-cooled board has no front panel; all PMC/XMC I/O signals are directed to the VPX backplane connectors.

The C112 in its conduction-cooled version is available in various mechanical formats and slot spacings: 0.8", 0.85", and 0.85" REDI.

Power Requirements

The C112 is designed to take its main power from 5 V (VS3) or 12 V (VS1 + VS2). When working from 12 V, the C112 still draws 2 A from the 5 V supply. When the C112 takes its main power from 5 V, no 12 V supply is required.

The C112 draws only 500 mA from 3.3 V_AUX.

The PMC site always draws power from the 5 V rail. The XMC site is provided with either +5 V or +12 V VPWR. The default power is 5 V.

All other power sources required by C112 resources are generated on board.

Total power consumption of the C112 depends on its configuration and assembly options.

Table 2. C112 Power Consumption

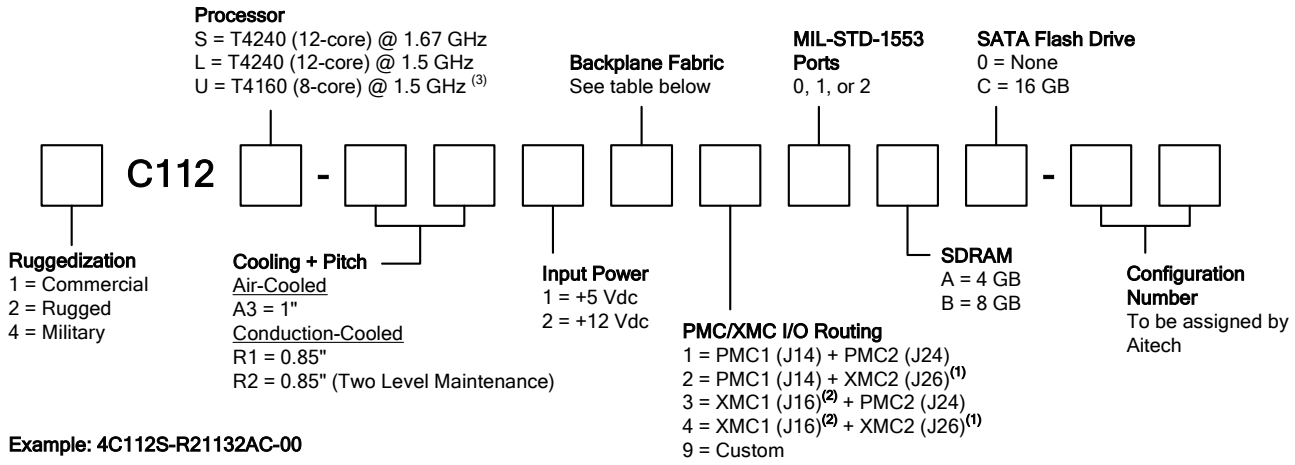
Processor	Typ	Max
T4240 @ 1.67 GHz	TBD	TBD
T4240 @ 1.5 GHz	TBD	TBD
T4160 @ 1.5 GHz	TBD	TBD

Environmental Features

Please refer to the Aitech Ruggedization datasheet.

C112
Freescale™ QorIQ™ T4 6U VPX SBC

Ordering Information



Example: 4C112S-R21132AC-00

Table 3. C112 Backplane Fabric Options

Option #	P1 (Data Plane)				P2 (Expansion Plane)	P4 (Control Plane)				P4/P6 (I/O)	VITA 65 Profile Name
	4-lane	4-lane	4-lane	4-lane		1000Base-KX		1000Base-T			
	DP1	DP2	DP3	DP4		CPutp1	CPutp2	CPtp1	CPtp2	Gb Port	
1	XAUI	XAUI	XAUI(3)	XAUI	4 PCIe x 4	Up to two ports in any combination				0	MOD6-PAY-4F2T-12.2.2-n
2(1)	PCIe/SRIO	PCIe(3)	0	0	4 PCIe x 4	1	1	1	1	2	MOD6-PAY-2F2U2T-12.2.5-n
9	Custom										

Notes:
1. When XMC2 I/O routing is chosen, GLAN3 is routed on behalf XMC2_IOA\B\D\E17 and XMC2_IOA\B\D\E19
2. When XMC1 I/O routing is chosen, SP7 differential clock lines are routed on behalf XMC1_IOA17 and XMC1_IOB17
3. When choosing T4160 QorIQ SOC, these interfaces will not be available.

For more information about the C112 or any Aitech product, please contact Aitech Defense Systems sales department at (888) Aitech-8 (248-3248).

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